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CALL FOR PAPERS

The Leading International Components, Packaging, and Manufacturing Technology Symposium

13th IEEE CPMT Symposium Japan

November 13 – 15, 2024,
Venue: Ritsumeikan University Suzaku Campus, Kyoto, JAPAN
(On-site only)
https://www.ieee-csj.org/

“Innovation of Packaging Technology for Advanced Heterogeneous Integration”

“IEEE CPMT Symposium Japan (ICSJ)” is one of the most widely recognized international conferences sponsored by the **IEEE Electronics Packaging Society (EPS)** and has been held annually in Kyoto in November. This conference was inaugurated in 1992 as “The VLSI Packaging Workshop in Japan (VPWJ)” to provide a platform for you to communicate and interact with global leaders in packaging technology. Later in 2010, this conference was renamed to “ICSJ” and ICSJ2024 is the 13th ICSJ meeting, or 22nd conference since establishing VPWJ.

Innovation of Packaging Technology for Advanced Heterogeneous Integration: Semiconductor devices have contributed to the development of various fields including PCs, because the pursuit of miniaturization (More Moore) has made it possible to simultaneously meet the demands for high speed, lower power consumption, and lower cost. On the other hand, the limit for miniaturization of silicon CMOS transistors is approaching and we are now pursuing a new axis of development called “More than Moore”, which is evolving in the direction of functional diversification. Indeed, heterogeneous integration is attracting attention as the key to the continued growth of the semiconductor industry. Integrating heterogeneous materials, devices, and circuits (e.g., analog/RF, passives, Si photonics, sensors/MEMS, biochips) into a 3D system-in-package is becoming widespread as the productivity driver. Furthermore, In the post-Moore’s Law era of the semiconductor industry, heterogeneous integration and chiplet-based approaches through the advanced 2.5D and 3D packaging technology such as a die-to-die (D2D), die-to-wafer (D2W), and wafer-to wafer (W2W) hybrid bonding will play a crucial role for high-end applications including high-performance computing (HPC), artificial intelligence (AI), servers, and data centers. In 2024, our focus is on key electronics packaging technologies for advanced heterogeneous integration and emphasizes on the following main topics: **Photonics, Advanced Packaging, Process & Material, Power & Automotive Electronics, Bioelectronics & Healthcare,** and **Signal/Power Integrity**. Additional topics of primary interest to the participants are listed below.

Other topics include (but not limited to):

+ Fine Pitch Assembly & Hybrid bonding
+ Packaging for Neuromorphic or Quantum computing
+ Laminated Materials & Processing
+ Co-packaged Optics & Materials for optical packaging
+ Packaging for High-Speed Electrical Interconnect
+ Signal Integrity & Power Integrity
+ RF Components & Modules
+ Additive Manufacturing & 3D Printed Electronics
+ Resilient Packaging for Autonomous System
+ Low Power, Low Temperature & Ultra Low Noise System Packaging

This conference is a perfect opportunity for you to communicate, interact, exchange technical ideas, and discuss your latest novel research findings in packaging technologies with experts from industry and academia. In addition

to the regular sessions, there is an "Early Career Researchers' (ECR)" session for young researchers with less than 2-year experience in their professions and all students including Ph.D. to hold fruitful communications with the experts. The ECR sessions will be held as a poster session. Authors are invited to submit an abstract through our website https://www.ieee-csj.org. **The abstract deadline is May 31, 2024**. Notification of acceptance will be sent by July 12, 2024, and the authors are requested to submit a 4-page manuscript by September 9, 2024 for the Technical Digest which will be available via **IEEE Xplore Digital Library**, whereas the authors for the ECR session are required to submit a 2-page manuscript.

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